IN THE CLAIMS

1-43. (Canceled).

44. (Currently Amended) A method of operating a semiconductor memory including dynamic memory cells, comprising the step of

entering a low power consumption mode, in which the dynamic memory cells do not retain data therein by prohibiting refresh operations, in response to a dedicated external control signal supplied from an exterior via a dedicated external terminal in order to control the low power consumption mode.

45. (Previously Presented) The method of operating a semiconductor memory according to claim 44, wherein

the semiconductor memory enters the low power consumption mode in response to a voltage change of the dedicated external control signal from a first voltage to a second voltage.

46. (Previously Presented) The method of operating a semiconductor memory according to claim 45, wherein

the low power consumption mode is maintained while the dedicated external control signal has the second voltage.

47. (Previously Presented) The method of operating a semiconductor memory according to claim 45, wherein

the semiconductor memory exits the low power consumption mode in response to a reverse voltage change of the dedicated external control signal from the second voltage to the first voltage.

48. (Currently Amended) A method of controlling a semiconductor memory including dynamic memory cells, comprising the step of

outputting a dedicated control signal to a dedicated external terminal in order to control a low power consumption mode made by the semiconductor memory so that the semiconductor memory enters a low power consumption mode, in which the dynamic memory cells do not retain data therein by prohibiting refresh operations.

49. (Previously Presented) The method of controlling a semiconductor memory according to claim 48, further comprising the step of

changing a voltage of the dedicated control signal from a first voltage to a second voltage when outputting the dedicated control signal.

50. (Previously Presented) The method of controlling a semiconductor memory according to claim 49, further comprising the step of

keeping the voltage of the dedicated control signal at the second voltage to maintain the low power consumption mode of the semiconductor memory.

51. (Previously Presented) The method of operating a semiconductor memory according to claim 50, further comprising the step of

changing the voltage of the dedicated control signal from the second voltage to the first voltage so that the semiconductor memory exits the low power consumption mode.

52. (Currently Amended) A memory system comprising:

a first memory including dynamic memory cells, having a low power consumption mode and a data terminal, the low power consumption mode being a mode in which the

dynamic memory cells do not retain data therein while power is on by prohibiting refresh operations, and ~~the first memory having a data terminal~~ the mode entered in response to a dedicated external control signal supplied from an exterior via a dedicated external terminal in order to control the low power consumption mode; and

a second memory including flash memory cells, having a data terminal which is connected with the data terminal of the first memory.

53. (Previously Presented) The memory system according to claim 52, wherein

data stored in the dynamic memory cells in the first memory is transferred to the flash memory cells in the second memory before the first memory enters the low power consumption mode.

54. (Previously Presented) The memory system according to claim 52, wherein

data stored in the flash memory cells in the second memory is transferred to the dynamic memory cells in the first memory after the first memory exits the low power consumption mode.

55. (Currently Amended) A cellular phone having a service state and a waiting state, comprising:

a first memory including dynamic memory cells, having a low power consumption mode, a data terminal, and an external terminal, the consumption mode being a mode in which the dynamic memory cells do not retain data therein while power is on by prohibiting refresh operations, and the ~~first memory having a data~~ external terminal being a terminal dedicated for receiving a dedicated external control signal to control the low power consumption mode; and

a second memory including flash memory cells, having a data terminal which is connected with the data terminal of the first memory, wherein

data stored in the dynamic memory cells in the first memory is transferred to the flash memory cells in the second memory then the first memory enters the low power consumption mode in response to the dedicated external control signal ~~upon~~ by shifting from the service state to the waiting state, and wherein

the first memory exits the low power consumption mode in response to the dedicated external control signal, and then data stored in the flash memory cells in the second memory is transferred to the dynamic memory cells in the first memory upon shifting from the waiting state to the service state.

56. (Currently Amended) A method of controlling a first memory including dynamic memory cells, having a low power consumption mode, a data terminal, and an external terminal, the consumption mode being a mode in which the dynamic memory cells do not retain data therein while power is on by prohibiting refresh operations, and the data terminal being a terminal dedicated for receiving a dedicated external control signal to control the low power consumption mode, and a second memory including flash memory cells, comprising the steps of:

transferring data stored in the dynamic memory cells in the first memory to the flash memory cells in the second memory before the first memory enters the low power consumption mode in response to the dedicated exterior control signal; and

transferring data stored in the flash memory cells in the second memory to the dynamic memory cells in the first memory after the first memory exits the low power consumption mode in response to the dedicated exterior control signal.